What is claimed is:

1. A digital signal receiver, comprising:

an equalizing unit which operates by a self-recovering equalization algorithm in an initial stage and by a decision directed equalization algorithm after a predetermined time has lapsed, for compensating for an amplitude distortion of a received signal;

an original signal decision unit for deciding an original signal from a signal which is compensated for the amplitude distortion;

a carrier recovering and phase lock detecting unit which operates after the predetermined time has lapsed, for detecting a phase error between an input of the original signal decision unit and the decided original signal, and outputting a phase lock signal when the phase is captured by the phase error;

a re-rotating unit for restoring the signal from the original signal decision unit to its original state by the phase compensated by the carrier recovering and phase lock detecting unit and outputting a restored signal to the equalizer; and

a coefficients updating unit for receiving the phase lock signal from the carrier recovering and phase lock detecting unit and the restored signal from the re-rotator unit, generating an error for updating the coefficients of the equalizer, and updating the coefficients of the equalizing unit.

2. The digital signal receiver of claim 1, wherein the equalizing unit comprises:

a feedforward equalizer;

a feedback equalizer;

an adder for adding the output from the feedforward equalizer to the output from the feedback equalizer; and

an equalization algorithm converter for selecting the output of the adder so as to be equalized by the self-recovering equalization algorithm in the initial stage, selecting the output from the re-rotator so as to be equalized by the decision directed algorithm when the phase lock signal is output from the carrier recovering and phase lock detecting unit, and outputting the selected output to the feedback equalizer.

3. The digital receiver of claim 2, wherein the output of the adder is limited to a fixed constant and below.

4. The digital signal receiver of claim 1, wherein the carrier recovering and phase lock detecting unit comprises:

a phase error detector for detecting a phase error between the input signal of the original signal decision unit and the decided original signal;

a phase lock detector for outputting the phase lock signal (Lock) when the phase is locked at the phase error detector and a frequency offset is within a predetermined range;

a phase locked loop for locking the phase when the phase of the phase error from the phase error detector is not locked;

a selector for selecting "1" or an output from the phase locked loop;

a multiplier for multiplying the signal from the equalizing unit to the signal from the selector; and

a counter for controlling the selector so that "1" or the output from the phase locked loop is selected according to the signal from the phase lock detector.

5. The digital signal receiver of claim 1, wherein the re-rotating unit comprises:

a conjugate complex number generator; and

a multiplier for multiplying a complex output number from the conjugate complex number generator by the output from the original signal decision unit.

6. The digital signal receiver of claim 1, wherein the coefficients updating unit comprises:

an error generator for receiving the outputs from the equalizing unit and the re-rotating unit and generating an error for updating the equalizing unit according to the signal from the equalizer in an initial stage and generating an error for updating the equalizing unit according to the signal from the re-rotating unit when the phase lock signal is received from the phase lock detector;

a first coefficients updater for updating the coefficients of the feedforward equalizer according to the error from the error generator; and

a second coefficients updater for updating the coefficients of the feedback equalizer.

7. The digital signal receiver of claim 3, wherein the phase locked loop increases loop bandwidth so as to quickly capture the frequency offset when the carrier recovering unit operates in the initial stage.

8. The digital signal receiver of claim 4, wherein the counter controls the selector by counting the number of symbols of the received signal.

9. A method for receiving a digital signal using a digital signal receiver including an equalizer for compensating for an amplitude distortion of a received signal, a carrier recovering unit for compensating for frequency offset of the received signal, and a phase

lock detector for comparing a signal in which the frequency offset is recovered with an output of an original signal decision unit, detecting an error value, and generating a frequency offset capture signal when the error value is no more than a predetermined threshold value and a frequency offset release signal when the error value is no less than the predetermined threshold value, comprising the steps of:

(a) determining whether the output from the phase lock detector is a frequency offset release signal or a frequency offset capture signal;

(b) compensating for the distortion of the received signal by not operating the carrier recovering unit and operating the equalizer by a self-recovering equalization algorithm when it is determined that the frequency offset release signal is output in the step (a); and

(c) compensating for the distortion of the received signal by operating the carrier recovering unit and operating the equalizer by a decision directed algorithm when it is determined that the frequency offset capture signal is output in the step (a).